



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,292	10/29/2003	Yang Kuao Kuo	N1085-00172	5133
8933	7590	05/03/2004	EXAMINER	
DUANE MORRIS, LLP IP DEPARTMENT ONE LIBERTY PLACE PHILADELPHIA, PA 19103-7396			BELLAMY, TAMIKO D	
			ART UNIT	PAPER NUMBER
			2856	

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/696,292

Applicant(s)

KUO, YANG KUAO

Examiner

Tamiko D. Bellamy

Art Unit

2856

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 October 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/29/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 560 (see fig. 7). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-30, 32, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Imai et al. (5,502,311).

With respect to claims 1, 10, and 19 Imai et al. discloses a light source (e.g., illuminating light IL) and a light detector (e.g., sensor array 15). Imai et al. discloses calculating deviation signals in accordance with the deviation amount of the planar surface (e.g., substrate surface) with respect to the reference plane (e.g., fiducial plane). Imai et al. discloses the signals from the light detector (e.g., sensor array 15) are sent to a detection circuit (17). The output (FS) from the detection circuit (17) shows a first signal value (e.g., zero level) when the planar surface (e.g., wafer surface) is matched with the reference plane (e.g., fiducial plane) (col. 13, lines 25-38, col. 16, lines 31-37); and the

Art Unit: 2856

output (FS) from the detection circuit (17) shows a second signal value (e.g. positive or negative level) when the planar surface (e.g., wafer W) is displaced above or below (col. 13, lines 20-28). With respect to the further limitations of claim 19, Imai et al. discloses first and second reflectors (e.g., mirrors 6,7).

With respect to claims 2, 3, 11, 12, 20, and 21, Imai et al. discloses a light source (e.g., illuminating light IL). The light source Imai et al. uses is inherently one selected from a laser or light emitting diode.

With respect to claims 4, 13, and 22 Imai et al. discloses a collimator (e.g., diaphragm 4).

With respect to claims 5, 6, 14, 15, 23, and 24 Imai et al. discloses the light detectors (e.g., sensor array 15) are photodiodes or phototransistors (col. 13, lines 4-9).

With respect to claims 7, 16, 25, and 29 as depicted in fig. 5, Imai et al. discloses a first peak value (e.g., zero value of F_s) when the planar surface (e.g., wafer surface) is matched with the reference plane (e.g., fiducial plane) (col. 13, lines 25-38, col. 16, lines 31-37).

With respect to claims 8, 17, 26, and 30 as depicted in fig. 5, Imai et al. discloses a second value (F_s) that is less than the peak output value.

With respect to claim 9, Imai et al. discloses that his invention applies to detecting plane positions of a substrate (e.g., a mask, reticle, wafer, etc.) (col. 1, lines 13-1).

With respect to claims 18 and 35, Imai et al. discloses that his invention applies to detecting plane positions of a substrate (e.g., a mask, reticle, wafer, etc.) (col. 1, lines 13-1). The reticle inherently includes a reticle holding well as claimed.

With respect to claim 27, Imai et al. discloses projecting beams to a given portion on a surface (see col. 12, lines 34-38).

With respect to claim 28, Imai et al. discloses that his invention applies to detecting plane positions of a substrate (e.g., a mask, reticle, wafer, etc.) (col. 1, lines 13-1). The reticle inherently includes a reticle holding well as claimed. Imai et al. also discloses a reflector (e.g., mirror 7) deflecting a reflected beam towards a light detector (e.g., sensor array 15).

With respect to claim 32, as depicted in fig. 1, Imai et al. discloses an optical level detector (e.g., illuminating light IL, projecting system PL, and sensor array 15) to adjust to surface of a reticle (e.g., wafer/reticle W) by way of a driving unit (22) to move the leveling stage (23) along the AX direction. Therefore, the height of the optical level detector (e.g., illuminating light IL, projecting system PL, and sensor array 15) is adjusted relative to the top of the reticle surface (e.g., wafer surface W).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 31, 33 and 34 are rejected under 35 U.S.C. 103(a) as being obvious over Imai et al. (5,502,311).

With respect to claim 31, Imai et al. discloses measuring points are set up in plural locations in the projection field to measure the positional deviation in the direction AX of the optical axis of a planar plane (e.g., wafer W) (col. 12, lines 34-38). Imai et al. also discloses a plurality of light detectors (e.g., sensor array 15). Imai et al. does not specifically disclose that four optical level detectors are set up near each of the four corners of a reticle holding well. However, as depicted in fig. 1, Imai et al. discloses a plurality of incident beams project toward the planar surface (e.g., wafer W); and the reflected beams are received by light detectors (e.g., an array of sensors 15). Furthermore, the device that Imai et al. can easily be manipulated project the incident beams toward four corners of a reticle holding well and the light detectors (e.g., array sensors 15) receive the reflected beams from the four corners. Therefore, to employ Imai et al. on a four level detectors mounted near four corners would have been obvious to one of ordinary skill in the art at the time of the invention since this reference explicitly teaches its use on detecting the plane position of a reticle which measures a plurality of locations on a projection field.

With respect to claims 33 and 34, as depicted in fig. 1, Imai et al. discloses an optical level detector (e.g., illuminating light IL, projecting system PL, and sensor array 15) to adjust to surface of a reticle (e.g., wafer/reticle W) by way of a driving unit (22) to move the leveling stage (23) along the AX direction. Therefore, the height of the optical level detector (e.g., illuminating light IL, projecting system PL, and sensor array 15) is

adjusted relative to the top of the reticle surface (e.g., wafer surface W). Imai et al. lacks the detail of a connecting hardware including an actuating guide bearing comprising wormgear teeth, a bed, and a worm. However, Imai et al. uses hardware that performs the same function as the claimed connection hardware. Furthermore, the use of connection hardware for the purpose of providing an adjustable component is a design consideration clearly within the preview of one having ordinary skill in the art.

Therefore, to employ Imai et al. on connection hardware including an actuating guide bearing comprising wormgear teeth, a bed, and a worm would have been obvious to one of ordinary skill in the art at the time of the invention since this reference explicitly teaches its use on detecting the plane position of a reticle and adjusting the stage of the reticle to correct the level variations of the reticle.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tamiko D. Bellamy whose telephone number is (571) 272-2190. The examiner can normally be reached on Mondays, Tuesdays & Fridays 6:30 AM to 3:30PM; and on Wednesdays and Thursdays the examiner 6:30 AM to 11:30 AM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hezron Williams can be reached on (571) 272-2208. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 10/696,292

Page 7

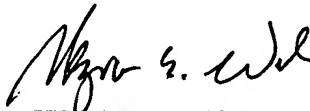
Art Unit: 2856

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tamiko Bellamy

T.B.

April 26, 2004



HEZRON WILLIAMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800